REMARKS

In the Claims:

Claims 9-16 remain in this application. Claims 1-8 and 17-20 have been canceled.

Rejections Under 35 U.S.C. 103(a):

Claims 9-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cha et al. (U.S. 6,303,418) (hereinafter "Cha") in view of Rotondaro et al. (U.S. 6,835,639) (hereinafter "Rotondaro"). The rejection should be withdrawn because the methods for forming transistors taught by the two references are incompatible and could not be combined to result in the methods recited in claims 9-12.

Cha teaches a method to form transistors by first forming dummy gate electrodes (Cha, Figure 2, reference number 6) and dummy gate insulators (Cha, Figure 2, reference number 5), forming spacers (Cha, Figure 3, reference number 9) adjacent the dummy structures, then removing the dummy structures to form trenches between the spacers (Cha, Figure 5, reference numbers 14 and 15). A polysilicon-metal gate electrode (Cha, Figure 9, reference numbers 17 and 19 on the left side) for the PMOS transistor and a metal gate electrode (Cha, Figure 9, reference number 19 on the right side) for the NMOS transistor are then formed within the trenches. Thus, Cha teaches a "replacement gate method" where a first dummy gate is formed then removed and replaced by the gate of the transistors.

Rotondaro, in contrast, teaches forming a first type of silicide in an NMOS region (Rotondaro, Figure 7, $TaSi_2$ on the left) and a second type of silicide in a PMOS region (Rotondaro, Figure 7, Pd_2Si on the right). Each of these silicides blanket their respective regions. Portions of the respective blanket silicide layers are removed to leave behind gate

electrodes (Rotondaro, Figure 8, col. 6, lines 46-63). Because portions of blanket layers are removed to leave gate electrodes behind prior to formation of spacers, etc., this is a "subtractive method" to form gate electrodes.

The "replacement gate method" of Cha is not compatible with the "subtractive method" of Rotondaro. The "replacement gate method" taught by Cha requires that the gate electrode first formed be a dummy gate electrode and be removed. The "subtractive method" of Rotondaro requires that the gate electrode first formed remain in place (otherwise, there would be no point to the formation of the blanket silicide layers). Since the gate electrode first formed can not be both left in place and removed, the two methods are incompatible.

Because the methods taught by Cha and Rotondaro are incompatible, one of skill in the art would not combine Cha and Rotondaro to result in the methods recited in claims 9-12. The rejections should be withdrawn.

Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cha in view of Brask et al. (U.S. 6,770,568) (hereinafter "Brask").

Under 35 U.S.C. 103(c), this rejection of claim 9 should be withdrawn. Subject matter that qualifies as prior art only under 35 U.S.C. 102(e) does not preclude patentability if the reference and the application were, at the time the application was made, owned by the same person or subject to an obligation of assignment to the same person (35 U.S.C. 103(c)). As stated in the Office Action at page 5, Brask qualifies as prior art under 35 U.S.C. 102(e). Brask is assigned to the Intel Corporation. The present patent application is also assigned to the Intel Corporation (as recorded on December 29, 2003 at Reel 14859, Frame 0790), and under the inventor's employment agreement, was subject to an obligation of assignment to the Intel Corporation. Thus, under 35 U.S.C. 103(c), Brask does not preclude patentability of the pending claims, and this rejection of claim 9 should be withdrawn.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on October 27, 2005.

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